

IN THE CLAIMS

1

2

1. (Cancelled)

1

2

3

4

2. (Currently Amended) The method of claim 1 wherein the
programmable at least a portion of the PLD chip is partitioned into a plurality of rows and
columns of logic array blocks (LABs).

1

2

3

4

5

6

3. (Currently Amended) ~~The method of claim 1~~ A method of verifying a
full-chip electronic design of a programmable logic device (PLD) chip, the method comprising:
partitioning the PLD chip into a plurality of blocks;
generating a block level RTL model of one of the plurality of blocks, wherein generating
a block level RTL comprises:
creating a block level schematic of an electronic design;
extracting a block Ram Bit Address(RBA) file from the block level schematic;
extracting a block level CRAM array from the block level RBA file; and
generating the block level RTL using the block level CRAM array;
generating a block level functional representation of the one of the plurality of blocks;
producing a full chip RTL model using the block level RTL model and the block level
functional representation; and
using the full chip RTL model for verification, simulation or debugging.

1

2

3

4. (Original) The method of claim 3 wherein the block level CRAM array
comprises absolute coordinates and RAM bit values for each CRAM bit.

1

2

3

4

5. (Currently Amended) The method of claim 4 wherein the CRAM
iscomprises at least one of EPROM, EEPROM, fuse, anti-fuse, SRAM, MRAM, FRAM, or
DRAM.

1

2

3

4

5

6

6. (Currently Amended) ~~The method of claim 1~~ A method of verifying a
full-chip electronic design of a programmable logic device (PLD) chip, the method comprising:
partitioning the PLD chip into a plurality of blocks;
generating a block level RTL model of one of the plurality of blocks, wherein generating
a block level RTL comprises:

7 creating a block level schematic of an electronic design;
8 generating a full chip schematic using a plurality of the block level schematics;
9 producing a full chip RBA file from the full chip schematic;
10 extracting block level RBA file from the full chip RBA file;
11 extracting a block level CRAM array from the block level RBA file; and
12 generating a block level RTL model using the block level CRAM array;
13 generating a block level functional representation of the one of the plurality of blocks;
14 producing a full chip RTL model using the block level RTL model and the block level
15 functional representation; and
16 using the full chip RTL model for verification, simulation or debugging.
17

1
2 7. (Original) The method of claim 6 wherein the block level CRAM array
3 comprises absolute coordinates and RAM bit values for each CRAM bit.

1
2 8. (Currently Amended) The method of claim 7 wherein the CRAM
3 iscomprises at least one of EPROM, EEPROM, fuse, anti-fuse, SRAM, MRAM, FRAM, or
4 DRAM.

1
2 9. (Currently Amended) The method of claim ~~4~~3 further including:
3 comparing the block level RTL model to the block level schematic before producing a
4 full chip RTL model; and
5 modifying the block level functional representation and the block level CRAM array if
6 the block level RTL is not equivalent to the block level schematic.

1
2 10. (Currently Amended) The method of claim ~~4~~3 wherein the PLD is a
3 complex programmable logic device ("CPLD"), programmable array logic ("PAL"),
4 programmable logic arrays ("PLA"), field PLA ("FPLA"), erasable PLDs ("EPLD"), electrically
5 erasable PLD ("EEPLD"), logic cell arrays ("LCA") or field programmable gate arrays
6 ("FPGA").

1
2 11. (Currently Amended) The method of claim ~~4~~3 wherein the
3 programmable logic device is embedded into ~~another~~an electronic device.

12. (Currently Amended) The method of claim 12~~1~~ wherein the ~~other~~ electronic device comprises programmable and non-programmable circuitry.

13. (Original) The method of claim 2 wherein the LAB comprises a plurality of one or more of the following sub-blocks: LE, LIM, LAB wide, LEIM, CRAM and DIM.

14. (Currently Amended) The method of claim 1~~3~~ wherein one or more of the plurality of blocks ~~are~~comprise digital signal processing blocks, input/output blocks, or memory blocks, ~~etc.~~

15. (Currently Amended) A data processing system for verifying a full-chip electronic design of a programmable logic device (PLD) chip, the data processing system including instructions for implementing the method of claim 1~~3~~.

16. (Currently Amended) A method of verifying a programmable region of an electronic design, the method comprising:

partitioning the programmable region into a plurality of blocks;

generating a block level RTL model of one of the plurality of blocks wherein generating a block level RTL comprises:

creating a block level schematic of an electronic design;

extracting a block Ram Bit Address(RBA) file from the block level schematic;

extracting a block level CRAM array from the block level RBA file; and

generating the block level RTL using the block level CRAM array;

generating a block level functional representation of the one of the plurality of blocks;

producing a full region RTL model from the block level RTL model and the block level functional representation; and

using the full region RTL model for verification, simulation or debugging.